We Claim:

1. A method, comprising:

obtaining, from within a memory system, information to indicate a data mask mapping scheme to be used in a memory module in the memory system; and

determining the data mask mapping scheme based on the information.

2. The method of claim 1, wherein said obtaining includes:

sending at least one instruction to the memory module directing the memory module to send the information; and

receiving the information from the memory module.

3. The method of claim 2, wherein said receiving the information from the memory module includes receiving the information from a serial presence detect within the memory module.

4. The method of claim 3, wherein said receiving the information from the serial presence detect includes receiving an indicator to indicate the data mask mapping scheme.

5. The method of claim 3, wherein said receiving the information from the serial presence detect includes receiving the data mask mapping scheme.

6. The method of claim 1, wherein:

said obtaining includes writing at least one test data mask pattern and at least one test data pattern to a range of memory in the memory module and reading at least one

resulting data pattern that was stored in the range of memory responsive to the at least one test data pattern being modified by the at least one test data mask pattern; and

said determining includes determining a portion of the data mask mapping scheme to be used for the range of memory based on the at least one resulting data pattern.

7. The method of claim 6, wherein said writing includes:

performing a first write transfer to write a first test data pattern to the range of memory; and

performing a second write transfer to the range of memory, the second write transfer including a second test data pattern and a test data mask pattern, the test data mask pattern to not write-protect a particular data chunk in the second test data pattern.

8. An apparatus, comprising:

a memory controller having a hardwired selection device to program the memory controller with a data mask mapping scheme, the data mask mapping scheme to associate at least one data mask bit with at least one data chunk in a memory module; and

an output to be coupled to the memory module.

9. The apparatus of claim 8, wherein the hardwired selection device is to receive the at least one data mask bit and at least a portion of the at least one data chunk.

10. The apparatus of claim 9, wherein the hardwired selection device is to select one of the at least one data mask bit to be associated with one of the at least one data chunk according to the data mask mapping scheme.

11. The apparatus of claim 8, wherein the hardwired selection device is to implement the data mask mapping scheme.

12. An apparatus, comprising:

a memory controller including a storage device having information to indicate a data mask mapping scheme for the memory controller; and

an output coupled to the memory module.

13. The apparatus of claim 12, wherein the storage device is loadable with the data mask map by software.

14. The apparatus of claim 12, wherein the storage device is loadable with the data mask map by BIOS.

15. The apparatus of claim 12, wherein the storage device is to include the information at manufacture time.

16. The apparatus of claim 12, wherein the information is to include at least one indicator to indicate the data mask mapping scheme.

17. The apparatus of claim 12, wherein the information is to include the data mask mapping scheme.

18. A system, comprising:

a memory module to use at least one data mask mapping scheme to associate at least one data mask bit with at least one data chunk;

a memory controller coupled with the memory module, the memory controller to be programmed with the at least one data mask mapping scheme used in the memory module.

19. The system of claim 18, wherein the memory module includes a first and a second memory rank to use at least one of the at least one data mask mapping scheme.

20. The system of claim 19, wherein the first memory rank is to use a different data mask mapping scheme than the second memory rank.

21. The system of claim 19, wherein the first memory rank is to use a same data mask mapping scheme as the second memory rank.

22. The system of claim 18, wherein the memory controller is to include a storage device to be programmed with one of the at least one data mask mapping scheme used in the memory module.

23. The system of claim 22, wherein the storage device is to be coupled with a selection device to select one of the at least one data mask bit to be associated with the at least one data chunk according to the data mask mapping scheme.

24. A machine-readable medium that provides instructions, which when executed by a machine, causes the machine to perform operations comprising:

obtaining, from within a memory system, information to indicate a data mask mapping scheme to be used in a memory module in the memory system; and

determining the data mask mapping scheme based on the information.

25. The machine-readable medium of claim 24, wherein said obtaining includes:

sending at least one instruction to the memory module directing the memory module to send the information; and

receiving the information from the memory module.

26. The machine-readable medium of claim 25, wherein said receiving the information from the memory module includes receiving the information from a serial presence detect within the memory module.

27. The machine-readable medium of claim 26, wherein said receiving the information from the serial presence detect includes receiving an indicator to indicate the data mask mapping scheme.

28. The machine-readable medium of claim 24, wherein:

said obtaining includes writing at least one test data mask pattern and at least one test data pattern to a range of memory in the memory module and reading at least one resulting data pattern that was stored in the range of memory responsive to the at least one test data pattern being modified by the at least one test data mask pattern; and

said determining includes determining a portion of the data mask mapping scheme to be used for the range of memory based on the at least one resulting data pattern.

29. The machine-readable medium of claim 28, wherein said writing includes:

performing a first write transfer to write a first test data pattern to the range of memory; and

performing a second write transfer to the range of memory, the second write transfer including a second test data pattern and a test data mask pattern, the test data mask pattern to not write-protect a particular data chunk in the second test data pattern.

30. The machine-readable medium of claim 28, wherein said determining the portion of the data mask mapping scheme includes identifying the particular data chunk in the second test data pattern based on the at least one resulting data pattern.